Notice of Allowability	Application No.	Applicant(s)	
	10/501,427	BREKELMANS ET AL.	
	Examiner	Art Unit	
	Thomas J. Hiltunen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *amendment filed 08/07/06*.

2. ☒ The allowed claim(s) is/are *2-6 and 8-12*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachm nt(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Summary of changes in this action

1. Claims 2-6, and 8-12 are allowed
2. Claims 1, and 7 have been canceled by Applicant

Allowable Subject Matter

Claims 1-8, and 11-16 are allowed.

The following is an examiner's statement of reasons for allowance:

With respect to claim 3, there was no prior art found that disclosed a differential inverter that has a bias control signal input to a PMOS transistor through a resistive means, and second bias signal input to a NMOS transistor through another resistive means. Yin (USPN 5,705,946) disclosed a level-shifting device in Fig. 4 that has two differential inverters that receive input and bias signals. However, there is no motivation to use a level-shifting device for differential inverter 49. There was no cited prior art that taught motivation for replacing Weekes et al.'s generic differential inverter 49, with Yin's level shifter. Additionally, Shin et al. (USPN 5,703) discloses CMOS differential inverters composed of NMOS and PMOS circuitry, also it can be seen that the bias control circuit is composed of resistors (see Fig. 6). However, it would not be reasonable to consider the drains of 21-22, and the drains of 41-42 as the control input of the differential inverter as required by the recited claim language. Upon updated search the reference of Whitworth (USPAPN 2003/0214319) was found, which discloses in Fig. 6 bias generating circuits (311, and 313) controlling the gates of NMOS

and PMOS transistors (332 and 320) through resistors (r1 and r2). However, bias generators 311 and 313 are responsive to supply voltages and not a control signal output from a voltage divider across differential outputs as recited in claim 3. Furthermore Whitworth's circuit lacks differential inputs, and differential outputs. There is no other prior art found that disclosed the recited language of claim 3, or provides motivation to combine the teachings of the prior. Thus claim 3 is allowable, and claim 2 is allowable for at least the same reasons as claim 3.

With respect to claim 4, There was prior art found that taught the using inverters to split a single input signal into two. However, there was no motivation provided by Weekes et al. to use the signal splitter in its bias circuit. For example Fig. 6 of Yamamoto et al. taught the using an inverter 38b to split a signal to two other inverters (40a and 40b), which are then input to a p and n type transistors 42 and 44. However, there is no motivation to use this type of buffer in place of that of buffer 48 in Weekes et al.. This is because 48 outputs a single signal which is split between two resistors, whereas Yamamoto et al. outputs two signals that are already split. There would be no motivation for adding more circuit components to Weekes et al., because it would be more expensive to manufacture and it would perform the same as the single buffer 48. Chiu et al (USPN 6,734,700) discloses the same situation as Yamamoto et al. in Fig. 1A, and it too doesn't supply any motivation to replace 48 of Weekes et al. with it. Additionally, Tang et al. (USPN 6,794,900) discloses a circuit that has two separate signals that are inverted being supplied to a differential input from the output through a two bias generators. However, these signals are not derived from a single bias signal,

which is voltage divided at the between the outputs. Rather, they are derived straight from each differential output. There is no motivation to voltage divide these signals to be input to a bias control. Therefore there would be no single bias signal to be sent to the signals splitters of Chiu et al. and Yamamoto et al. Thus, claim 4 is allowable, and claim 5 is allowable for at least the same reasons as claim 4.

With respect to claim 6, there was no prior art found that taught a differential amplifier with an "LC tank" coupled to its outputs and then feedback to the inputs of the differential inverter. There was prior art found that did have a differential inverter with an LC tank between its outputs, such as Fig. 1 of Smith et al. (USPN 6,043,710), Fig. 6 of Horiguchi et al (USPN 5,952,856), and Fig. 9 of Sugawara (USPN 5,495,194). Also, there was no prior art found that provided motivation for combining claim the teachings of Weekes et al. with the any of the cited prior art with LC tanks. No cited prior taught the further recitation a differential inverter having its outputs connected to a LC and cross-coupled to the input of the inverter. Thus, claim 6 is allowable.

With respect to claims 8-12, it can be seen that claims 8-12 essentially recite the same limitations as claims 2-6 with "American-style claim language". Thus claims 8-12 are allowed for at least the same reasons as claims 2-6.

Applicant's assumption that "the reference to 35 U.S.C § 112 on page 4 of the Office Action is an inadvertent vestige of a similar reference in the Office Action dated September 30, 2005" is correct. There is no rejections under 35 U.S.C § 112 in the office action dated May, 5 2006, and Applicant's amendment filed March 3, 2006 overcame all previous rejections under 35 U.S.C § 112.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas J. Hiltunen whose telephone number is (571)272-5525. The examiner can normally be reached on Mondays - Fridays from 8:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan, can be reached on (571) 272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH
August 16, 2006

LINH MY NGUYEN
PRIMARY EXAMINER